Claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by Asano et al. (U.S. Patent No. 4,612,462, "Asano"). However, Applicants respectfully submit that claim 1 recites subject matter that is neither disclosed nor suggested in Asano.

Claim 1 recites a level shift circuit that includes a capacitor and a charge control circuit connected to the capacitor for providing a voltage of a high potential power supply to the capacitor and controlling charging of the capacitor. A limiting circuit is connected to the high potential power supply and the charge control circuit for limiting the voltage provided to the capacitor from the high potential power supply, before the charge control circuit stops providing the voltage of the high potential power supply to the capacitor.

In making this rejection, the Office Action took the position that Asano discloses all of the elements of the claimed invention. However, it is respectfully submitted that the prior art fails to disclose or suggest the structure of the claimed invention, and therefore, fails to provide the advantages of the present invention. For example, the shift level circuit of the present invention includes a capacitor and a charge control circuit connected to the capacitor that provides a voltage of a high potential power supply to the capacitor and also controls the capacitor. A limiting circuit is connected to the high potential power supply and the charge control circuit for limiting the voltage provided to the capacitor from the high potential power supply, before the charge control circuit stops providing the voltage of the high potential power supply to the capacitor.

As a result of this claimed configuration, when the capacitor performs voltage step-up, the current limiting circuit limits the charge that leaks from the capacitor to the

high potential power supply and increases the voltage step-up efficiency. This improves the response of the output signal in the level shift circuit.

The present invention is directed to a level shift circuit that includes a limiting circuit connected to a high potential power supply and a charge control circuit. The limiting circuit limits the voltage provided to a capacitor from the high potential power supply before the charge control circuit stops providing the voltage of the high potential power supply to the capacitor. That is, the limiting circuit is turned off before the charge control circuit is turned off.

Asano discloses a logic circuit that includes a voltage booster (15). The voltage booster (15) includes a capacitor (14), MOS transistors (81, 83), and an inverter (13). When an input signal goes to logical level "1," the MOS transistors (81, 83) turn on at the same time in response to an output signal of the inverter (13) and provide a boosted voltage (VH) from a boosted voltage retention circuit (70) to a signal output end B (capacitor (14)). When the input signal goes to logical level "0," the MOS transistors (81, 83) turn off at the same time in response to the output signal of the inverter (13).

The Office Action asserted that the MOS transistor (81) of Asano corresponds to the limiting circuit of the present invention and the MOS transistor (83) of Asano corresponds to the charge control circuit of the present invention. However, Asano does not disclose that the MOS transistor circuit (81) limits the voltage provided to the capacitor (14) when voltage booster (15) performs voltage step-up. In other words, Asano only discloses that the MOS transistor (81) provides the boosted voltage (VH) to the capacitor (14) when the voltage booster (15) performs voltage step-up. This is

contrary to the present invention where a limiting circuit is connected to the high potential power supply and the charge control circuit for limiting the voltage provided to the capacitor from the high potential power supply, before the charge control circuit stops providing the voltage of the high potential power supply to the capacitor.

Therefore, it is respectfully submitted that the Applicants' invention, as set forth in claim 1, is not anticipated within the meaning of 35 U.S.C. § 102.

Newly added claim 36 is directed to a level shift circuit including a capacitor. A first transistor is connected to the capacitor for providing a voltage of a high potential power supply to the capacitor, and for controlling charging of the capacitor. A second transistor is connected to the high potential power supply and the first transistor. The second transistor is turned off before the first transistor is turned off. Asano fails to disclose or suggest the second transistor. Claims 37-49 are dependent upon claim 36, and claims 40-42 are dependent upon claim 1. Therefore, it is respectfully submitted that the newly-added claims are patentable over the applied references.

In view of the foregoing, reconsideration of the application, withdrawal of the outstanding rejections, allowance of claims 1 and 36-42, claims 2-10 already being allowed, and the prompt issuance of a Notice of Allowability are respectfully solicited.

Should the Examiner believe anything further is desirable in order to place this application in better condition for allowance, the Examiner is requested to contact the undersigned at the telephone listed below.

In the event this paper is not considered to be timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an

extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 108075-00054.**

Respectfully submitted,
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